1877 Multihit Time-to-Digital Converter

- High Density, 96 Channels Per FASTBUS Slot
- 500 psec LSB
- Programmable Full Scale up to 32 µsec
- Up to 16 Hits/Channel (Programmable)
- Rising and/or Falling Edge Timing Information
- < 20 nsec Double Pulse Resolution
- Fast Conversion
- Built-in Data Zero Suppression and Data Compaction
- Multiple Event Buffer, 7 Events
- High-Speed FASTBUS Block Transfers
- Supports the Multi-Module Data Transfer Specification (Multi-Block)
- Built-in Self Test

HIGH RATE TDCs FOR WIRE CHAMBER SPECTROMETERS

The FASTBUS Model 1877 is a 96-channel, high resolution, multihit TDC designed for high rate experiments. This TDC provides precise time measurements for spectrometers and hodoscopes consisting of multiwire propor tional, drift or time projection chambers. With a least count of 500 psec and a 16-bit range, the Model 1877 can measure time intervals up to 32 µsec duration. The instrument operates in Common Start or Common Stop modes. Common Stop Mode eliminates the need for expensive delay cables normally required for each input channel of a fixed target experiment.

The 1877 provides the high performance, high density, versatility, and automated test features required for large scale experiments. By using the FASTBUS standard, the LeCroy 1800 family of data acquisition modules is one of the most sophisticated data acquisition systems today.

FUNCTIONAL DESCRIPTION

Input Circuits

The individual channel inputs are located on the front panel. They accept differential ECL signals and are termi nated in 110 ohm. The COMMON input (Common Start or Stop) also accepts ECL signals and has a removable 110 ohm termination. By removing this termination, the COMMON signal(s) can be cascaded, as long as the termination in the last module of a block of modules is left in place. This scheme eliminates the extra propagation delays caused by embedded repeaters and leaves only the very slight delays due to the cables cascading the individual modules (approximately 50 psec/cm).

Conversion Technique

At the heart of the 1877 lies the MTD133B Monolithic Time Digitizer, an 8-channel, 16-bit dynamic range TDC circuit with 500 psec least count. Arrival times can be recorded for either the rising, falling or both edges. The double pulse resolution is 20 nsec.

The MTD133B uses a high-speed clock, a continuously counting scaler, and four state interpolators. When a pulse arrives, the contents of the scaler and interpolator are stored in memory. Up to 16 words of data can be stored in the LIFO (Last In First Out memory) for each channel. During readout each of the stored signal times is automatically subtracted from the COMMON hit time. Therefore, the output is the actual time difference with virtually no pedestal. The difference value is further compared to a programmable upper threshold and discarded if it is greater than this threshold. This threshold is programmable from 8 nsec to 32 µsec with a resolution of 8 nsec.

In this way the MTD133B accommodates many different, difficult measurement scenarios. For users who wish to detect only pulses coming within the drift time of the chamber, the programmable threshold produces a program mable full scale. In addition, the user can program the depth of the LIFO from 1 to 16 hits, thus creating a guaran teed maximum conversion time.

Control

Control registers configure the TDC to report either the time of the rising edges, falling edges or both, facilitating pulse width measurements. Test functions allow verification of each channel's behavior. Full scale time out in the COMMON START mode can either be programmed or supplied externally. Compatibility with the Model 1810 Calibration and Timing Module is maintained for COMMON START/STOP, fast clear, fast clear window, and test pulse distribution.

Multiple Event Buffering

The module contains a seven event buffer. This digital memory buffer provides two primary advantages. First, dead time in the experiment is reduced because data readout can be done during the acquisition of subsequent events. Second, the event data can be stored temporarily while the trigger decision to read or discard the event is made. Events in the buffer are discarded with a FASTBUS command to skip the event. This skip command causes an internal pointer to increment, positioning the next event at the top of the readout queue. As each event is recorded, a modulo eight event tag number is appended to it in order to allow the coherence across multiple modules to be verified.

FASTBUS Readout

The 1877 complies with the FASTBUS Standard (ANSI/IEEE-960). FASTBUS functions allow remote control and operation of the 1877. Data from the 1877 is automatically zero suppressed. Readout is in a FIFO-like manner, consisting of a header word followed by a variable number of data words. Channel identification information is appended to each data word.

The modules may be read out via a LeCroy Model 1821 FASTBUS Segment Manager/Interface (SM/I) at data transfer rates up to 10 Mwords/sec. In addition, the Model 1877 is compatible with the LIFT (LeCroy Interactive FASTBUS Toolkit) software package.

Applications

The Model 1877, 96-input TDC, has been designed to be as compatible as possible with the popular Model 1879 Pipelined TDC. With its shorter conversion time, higher precision and larger dynamic range, the 1877 is the perfect replacement for the 1879 in high rate, high accuracy applications.

By capturing both the rising and falling edge time information, the Model 1877 can be used in a "time-over -threshold" technique to simultaneously determine the time and total charge collected or, in some cases, the time and peak value for a given detector element using only one channel of TDC electronics. This technique avoids, at a greatly reduced cost, many of the traditional problems encountered with other methods, such as amplitude saturation.

Model 1877 Block Diagram

SPECIFICATIONS

Inputs: 96 ECL differential line receivers. Input impedance 110 ohm ±10%. Minimum pulse width 10 nsec FWHM (must be > 1 time bin width). Input swing 400 mV, differential.

Least Significant Bit: 500 psec.

Total R.M.S. Error: 400 psec (Note: The R.M.S. of a gaussian distribution is equal to sigma).

Time Out: Differential ECL input to mark the end of acquisition in COMMON START mode.

Full Scale: 0 to 32.768 µsec, ±0.0025%; programmable via CSR18 in steps of 8 nsec.

Pedestal: 14 to 20 counts.

Double Edge Resolution: The 1877 can measure two edges separated by as little as 10 nsec. No two pulse edges should be closer than 10 nsec. This implies a lower limit on the double pulse resolution of 20 nsec.

Common Start/Stop: From the Model 1810 CAT via TR6 line or from front-panel differential ECL input. CSR selected.

Fast Clear Window Input: From the Model 1810 CAT via TR5 line.

Fast Clear Window (FCW): Starts at end of Time Range (Common Start) or at Common Stop. Can be pro grammed 1024 nsec to 512 µsec. During this period, the user can apply a FAST CLEAR to discard the event just captured.

Zero Suppression: Automatic for channels that have no hit.

Long Term Stability: < 100 ppm/year.

Temperature Coefficient: < 10 ppm/°C.

Differential Non-Linearity: Maximum ±0.2 LSB (typical).

Integral Non-Linearity: < 25 ppm full scale.

Fast Clear: Differential ECL input via a 2-pin front-panel connector (removable termination resistors) or via backplane TR0 line. Minimum pulse width 40 nsec.) When applied during the FCW, clears data in the current event and readies module for acceptance of a new event. Fast clear settling time is < 250 nsec. Fast Clear is leading edge sensitive and must be performed during FCW.

Time Out: Differential ECL input via a 2-pin front-panel connector. Minimum width 50 nsec. In Common START mode, terminates measurement in progress and starts conversion.

Busy Output: Differential ECL output via a 2-pin front-panel connector. Indicates the module is converting hit information. The unit is unavailable for data capture.

Conversion Time: 750 nsec + 50 nsec per hit within the programmed full scale; 1.6 µsec minimum.

On-Board Tester: The tester generates square wave pulses (50% duty cycle). The pulse trains can have 1, 2, 4 or 8 cycles with half periods of 125, 250, 1000 nsec or 2000 nsec.

Multiple Event Buffer: The digital data memory is logically organized as a circular buffer, large enough to store the results of up to 7 events when used appropriately. One buffer is always dedicated for FASTBUS readout.

GENERAL

Front-Panel Indicators: Slave: Indicates module is being addressed. COMMON: Indicates whether Common Start/Stop was hit.

Power Requirements: 5 V at 5.0 A, -5.2 V at 4.0 A, -2 V at 3.0 A, 15 V at 100 mA, -15 V at 100 mA.

Packaging: Single-width FASTBUS module (ANSI/IEEE-960-1989).

FASTBUS CONTROL

Module Identification Code: Read Only, 103Ch.

Implemented Addressing Modes: Logical (16 bits), Geographical, Broadcast.

AS-AK Handshake Time: 125 nsec typical, 150 nsec maximum.

DS-DK Handshake Time: 65 nsec typical, 75 nsec maximum (Block Transfer).

Implemented Broadcast Functions:

(01)h - General Broadcast Select: The TDC modules are selected and respond to subsequent data cycles.

(05)h - Class N Broadcast: The TDC modules of Class N (programmed via CSR7) respond to subsequent data cycles.

(09)h - Sparse Data Scan (SDS): TDC modules containing one or more buffered events assert their "T pin" on the following read data cycle.

(19)h - Device Available Scan (DAS): TDC modules respond by asserting "T pin" if no events are buffered.

(0D)h - All Device Scan: All TDC modules assert their T pin on the following read data cycle.

(BD)h - AFC SDS: All TDC modules with AFCs requiring service assert their T pins.

(CD)h - TDC DS: TDC modules assert T pin if current event contains a non-zero number of data words.

** An h subscript denotes a hexadecimal number, i.e., base 16.*

Slave Status Responses to Data Cycles:
SS Significance

0 = Valid action.

2 = End of data.

3 = Error: Error in token pass during multi-module data scan.

7 = Error. Invalid secondary address loaded into internal address register.

DSR0 Output Word Bit Definitions

HEADER FORMAT

When logical addressing is enabled use top configuration.
When logical addressing is disabled use bottom configuration.

DATA FORMAT

D = Data
S = Edge: Rising Edge = 0, Falling Edge = 1 (on "+" inputs)
A = Channel number 0 - 95
G = Geographic address
L = Logic address
P = Parity
W = Word Count
B = Buffer

AUXILIARY CONNECTOR

Auxiliary Functions Card Socket - *Viewed From Front of Crate (Reverse for Rear View)*

Auxiliary Connector Pin Out Description

Trigger Bits: TTL, active low signals. Front-panel signals are converted to TTL and routed to Auxiliary Connec tor.

Trigger Strobe: A signal received by the TDC via the FASTBUS segment from the 1810 CAT module. Normally used by the AFC to define the fiducial time interval.

Aux_DB0* - Aux_DB11*: A 12-bit bidirectional bus. TTL, active low.

Aux RDB: Defines direction of data bus Aux_DB0-11. When high AFC is in read mode (i.e., being read from the Segment).

Aux WCLK*: All read/write clock applied to auxiliary card whenever the user accesses the user CSR space C0000000-C000000Fh.

Address Lines: CSR_ADR 0-3; Address lines CSR_ADR 0-3 in conjunction with the decode AFC address strobe (Aux WCIK*) allows user implementation of FASTBUS CSR locations C0000000 to C000000Fh. Sixteen locations are available for use on the AFC. CSR_ADR 0-3 are latched on 1877 card.

V_Addr*: TTL active low signal to be driven by AFC circuits if an implemented address is being accessed on the AFC. Used to generate the proper SS = 0 response to FASTBUS; otherwise, SS = 7 is generated if Valid Address is not driven low.

PCT*: TTL active low signal asserts module T pin in response to a (BD) h broadcast.

FC*: TTL active low signal equal in duration to the Fast Clear input applied via the front panel or 1810 CAT module.

Power Supply: All FASTBUS voltages.

** Indicates a low true signal.*